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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,134	07/08/2003	Waldemar Brinkis	502901-155	8115

7590 01/22/2007

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EXAMINER	
RODELA, EDUARDO A	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,134	BRINKIS ET AL.	
	Examiner	Art Unit	
	Eduardo A. Rodela	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Election response filed November 13, 2006. Group I (claims 1-12) has been elected.

Information Disclosure Statement

The information disclosure statement filed July 8, 2003 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because several foreign patent documents referenced have not been translated to English. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of power and/or electronic components of claims 1, 7, 8-10, and 12 (also the details of the stacked orientation of this claim), must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattman et al. (EP 1 249 869) in view of Asai et al. (US 4,521,476) and Liederbach (US 3,714,709).

Regarding claim 1, Mattmann shows an electronics unit, comprising:

a low multi-point metallic mount [1];

an insulating layer [2] arranged on said mount;

a conductor track system [4,5,6,7, which is a thick film type conductor, see English abstract] on said insulating layer [2]; and

electronic power components [9, it is well known to use several power devices in a single circuit or system, see elements 66 of Figure 14 of Morita et al. (Us 2002/0074651)] arranged on said conductor track system [4,5,6,7]. Mattmann does not show an insulating layer comprises a sintered electrically insulating polymer layer and also does not specify the conductor track system is comprised of a sintered glass frit with a noble metal filling. Asai shows (e.g. Figures 5-8) an insulating layer comprises a sintered [it is well known in the art that epoxies are cured by the application of heat, see line 7 of paragraph 0030 of Sakamoto et al. (US 2002/0020554)] electrically insulating polymer layer [1, which is used to connect conductor tracks 3' to metal base 8]. Asai teaches the benefits of having an insulating layer which is comprised of a sintered electrically insulating polymer layer as a material which can be used to permit high heat conductivity [column 2: line 60 to column 3: line 4]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the insulating layer comprising a sintered electrically insulating polymer layer arranged on said mount in the invention of Mattman as suggested by Asai because the insulating layer can be used to permit high heat conductivity. Liederbach shows an electronic system which has a conductor track system [4,6,8,10,12,14] is comprised of a sintered glass frit with a noble metal filling [column 3: lines 8-31]. Liederbach teaches the benefit of using a conductor track system is comprised of a sintered glass frit with a noble metal filling to

allow for screen printing pattern transfer [column 2: lines 55-65]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the conductor track system is comprised of a sintered glass frit with a noble metal filling in the invention of Mattmann as suggested by Liederbach to allow for screen printing pattern transfer.

Regarding claim 2, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. Liederbach, wherein said noble metal filling comprises one of a silver filling and a filling containing silver [column 3: lines 8-31].

Regarding claim 3, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. In addition, Liederbach shows wherein said glass frit is a low melting-point glass frit [shows the use of borosilicate glass frit, column 3: lines 22-27, which is well known to be a low melting point glass, see column 7: lines 18-27 of Pryor et al. (US 4,821,151)].

Regarding claim 4, Mattmann in view of Asai and Liederbach show the electronics unit of claim 2. In addition, Liederbach shows wherein said glass frit is a low melting-point glass frit [shows the use of borosilicate glass frit, column 3: lines 22-27, which is well known to be a low melting point glass, see column 7: lines 18-27 of Pryor et al. (US 4,821,151)].

Regarding claim 5, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. In addition, Mattmann shows wherein said mount [1] is

made of a material from the group consisting of aluminum and an aluminum alloy [see English abstract].

Regarding claim 6, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. In addition, Mattmann shows wherein said mount [1] comprises cooling ribs [protrusions on bottom surface].

Regarding claim 7, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. In addition, Mattmann shows wherein said power components [3] comprise at least one of power semiconductor elements and driver components [see English abstract].

Regarding claim 8, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. In addition, Mattmann shows comprising at least one of electrical and electronic components [9] arranged on the conductor track system [between 6 and 7].

Regarding claim 9, Mattmann in view of Asai and Liederbach show the electronics unit of claim 8. In addition, Mattmann shows wherein said power components [3] and said at least one of electrical and electronic components [9] are conductively connected to the conductor track system by bonding [both are bonded to conductor tracks 4,6,7].

Regarding claim 10, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. In addition, Mattmann shows wherein said power components [3] and said at least one of electrical and electronic components [9] are

conductively connected to the conductor track system by bonding [both are bonded to conductor tracks 4,6,7].

Regarding claim 11, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. In addition, Asai shows wherein said electrically insulating polymer layer [1] has a thickness of about >20 um [column 4: lines 52-55].

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mattman et al. (EP 1 249 869) in view of Asai et al. (US 4,521,476) and Liederbach (US 3,714,709) in further view of Akram (US 6,417,027).

Regarding claim 12, Mattmann in view of Asai and Liederbach show the electronics unit of claim 1. Mattmann, Asai, and Liederbach do not show:

a further insulating layer comprising a sintered polymer arranged on said conductor track system and on said electronic power components; a further conductor track system comprising a sintered glass frit with noble metal filling arranged on said further insulating layer; and further electronic power components arranged on said further conductor track system. Akram shows (e.g. Figures 1-4 and 8) a further insulating layer comprising a sintered polymer [insulator portion of 12, column 4: lines 23-35, uses polyimide, which is well known as a thermosetting material, see column 9: lines 24-29 of Meissner et al. (US 5,264,326)] arranged on a conductor track system [25] and on electronic power components [14]; a further conductor track system [portion of 12, made of conductive polymer thick film, column 4: lines 46-52]; and

further electronic power components [14, column 4: lines 15-25] arranged on said further conductor track system [12]. Akram teaches the benefits of stacking insulators,

conductor tracks, and extra devices to facilitate high density stacking of semiconductor devices [column 1: lines 15-18] as suggested by Akram. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the further insulating layer comprising a sintered polymer arranged on said conductor track system and on said electronic power components; a further conductor track system arranged on said further insulating layer; and further electronic power components arranged on said further conductor track system in the invention of Mattmann in view of Asai and Liederbach as suggested by Akram in order to facilitate high density stacking of semiconductor devices. Akram does not show the specific constituents of the polymer thick film conductor track system. However, Liederbach discloses that sintered glass frit with a noble metal filling is a known material for conductive polymer thick films. The applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571) 272-8797. The examiner can normally be reached on M-F, 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eduardo A. Rodela
Examiner

E.R.